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Intel® 82803AA Memory Repeater Hub for RDRAM (MRH-R)

Specification Update

March 2001

Document Number: 298181-002

Specification Update

intel.

Intel® 82803AA MRH-R

Contents

Revision History

Rev.	Draft/Changes	Date
-001	Initial Release	March 2000
-002	Formatting changes only. No technical information changes	March 2001

Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents/Related Documents

Document Title	Document Number
Intel® 82803AA *Memory Repeater Hub for RDRAM (MRH-R)* datasheet	298022-002

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the Intel® 82803AAMRH-R behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Marking Information

The Intel® 82803AA MRH-R may be identified by the following component markings:

Stepping	S-Spec	Top Marking	Notes
A-2	SL3ML	FW82803AA, SL3ML	

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes which apply to the listed Intel® 82803AA MRH-R steppings. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This item is either new or modified from the previous version of the document.

NO.	A2	SPECIFICATION CHANGES
1	X	Correction of 82803AA MRH-R Auto Levelization Process

Number	Steppings	Plans	ERRATA
	A2		
1	X	NoFix	82803AA MRH-R SMBus Controller
2	X	NoFix	82803AA MRH-R IRO Bit
3	X	NoFix	82803AA MRH-R Single Channel Powerdown

Number	SPECIFICATION CLARIFICATIONS
	There are no specification clarifications in this Specification Update revision

NO.	A2	DOCUMENTATION CHANGES
1	X	82803AA MRH-R ST—Stepping Register

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Specification Changes

1.   **Correction of 82803AA MRH-R Auto Levelization process**

The 'Stick' Channel Time Domain delay is programmed via the tRDLY_stick bits[2:0] in the 82803AA MRH-R LMTR register.

The 82803AA MRH-R updates this delay during the levelization process by measuring on-the-fly, the number of rclks from an expansion SCP read command to the first non-zero data seen on 'stick' channel signal DQA5 at the 82803AA MRH-R. This automatic process is being de-featured.

The correct method of levelizing 'stick' channel B is documented in the Intel® 82840 MCH BIOS Specification.

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Errata

1.   82803AA MRH-R SMBus Controller

Problem: The SMBus controller in the 82803AA MRH-R will fail intermittently when reading data from RDRAM devices.

Implication: BIOS algorithms that use the 82803AA MRH-R SMBus controller to detect memory will encounter unreliable results. This can cause the BIOS to hang during boot time. The 82803AA MRH-R SMBus controller should not be used.

Workaround: The ICH SMBus controller should be used in place of the 82803AA MRH-R SMBus controller. Careful attention should be given to selecting SMBus addresses to avoid address contention when making this change.

Status: There are currently no plans to fix this erratum.

2.   82803AA MRH-R IRO Bit

Problem: The 82803AA MRH-R does not clear the IRO bit (Initiate RIC Operation) after issuing the SET Fast clock command. The BIOS will check this bit for completion of the SET Fast clock command.

Implication: This will result in a system hang if the BIOS uses this bit to determine a SET Fast clock command completion.

Workaround: No workarounds are required. The 82803AA MRH-R will issue the SET Fast clock command within 1 SCLK of the IRO bit being set in the RIC register. The time necessary to program the RIC register with another command is greater than 1 SCLK.

Status: There are currently no plans to fix this erratum.

3.   82803AA MRH-R Single Channel Powerdown

Problem: The MCH will issue a powerdown entry command to each individual stick channel that will power down the devices, MRH-R clocks and RAC on the targeted stick channel. Upon the receipt of an individual stick channel powerdown command, the 82803AA MRH-R will power down the MRH-R clocks and RACs on the intended stick channel as well as the unintended one.

Implication: The stick channel that did not receive the powerdown command will be inaccessible to proper powerdown entry commands. The improper powerdown will result in the loss of data content on that channel. The system will not be able to return from *Suspend-to-RAM* properly.

Workaround: The MRH-R will set the RC bit after both the expansion and slave RACs have been initialized. The BIOS should write a '1' to the RC bit (MRH-R RIR Register at 0Fh, bit 4) after it is set by the MRH-R.

Status: There are currently no plans to fix this erratum.

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Specification Clarifications

There are no specification clarifications in this Specification Update revision.

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Documentation Changes

1. **82803AA MRH-R ST—Stepping Register**

ST-Stepping Register, High Word
Address: 24h
Default: 0002h
Access: Read Only
Size: 16 bits

Bit	Description
15:8	**Reserved**
7:4	**Protocol Revision.** This field specifies the version of the Direct RDRAM channel implemented.
3:0	**Revision Identification Number.** This is a 4 bit field that identifies the revision identification number for the MRH-R. For A-2 stepping the value is 010h