March 1998

## FAIRCHILD

# DM74LS74A Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs

#### **General Description**

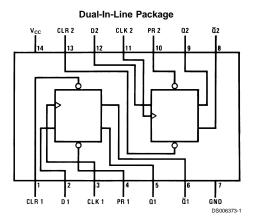
This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is low or high without affecting the outputs as long as the data setup and

hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

#### Features

 Alternate military/aerospace device (54LS74) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

### **Connection Diagram**



Order Number 54LS74DMQB, 54LS74FMQB, 54LS74LMQB, DM54LS74AJ, DM54LS74AW, DM74LS74AM or DM74LS74AN See Package Number E20A, J14A, M14A, N14A or W14B

#### **Function Table**

	Inp	uts	Outputs		
PR	CLR	CLK	D	Q	Q
L	н	Х	Х	н	L
н	L	X	X	L	н
L	L	x	x	H (Note 1)	H (Note 1)
н	н	↑	н	н	L
н	н	$\uparrow$	L	L	н
н	н	L	X	Q	$\overline{Q}_{0}$

H = High Logic Level

X = Either Low or High Logic Level L = Low Logic Level

↑ = Positive-going Transition

Q0 = The output logic level of Q before the indicated input conditions were established.

Note 1: This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (high) level.

Absolute	Maximum	Ratings (Note 2)
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Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	

DM54LS and 54LS	
DM74LS	
Storage Temperature Range	

#### -55°C to +125°C 0°C to +70°C -65°C to +150°C

## **Recommended Operating Conditions**

Symbol	Parameter		1	DM54LS74A			DM74LS74A		
			Min	Nom	Max	Min	Nom	Max	1
V <sub>cc</sub>	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
VIH	High Level Input	Voltage	2			2			V
V <sub>IL</sub>	Low Level Input \	/oltage			0.7			0.8	V
I <sub>OH</sub>	High Level Outpu	t Current			-0.4			-0.4	mA
I <sub>OL</sub>	Low Level Output	Current			4			8	mA
f <sub>CLK</sub>	Clock Frequency	(Note 4)	0		25	0		25	MHz
f <sub>CLK</sub>	Clock Frequency	(Note 5)	0		20	0		20	MHz
tw	Pulse Width	Clock High	18			18			
	(Note 4)	Preset Low	15			15			ns
		Clear Low	15			15			]
tw	Pulse Width	Clock High	25			25			
	(Note 5)	Preset Low	20			20			ns
		Clear Low	20			20			1
t <sub>su</sub>	Setup Time (Note	es 3, 4)	20↑			20↑			ns
t <sub>su</sub>	Setup Time (Notes 3, 5)		25↑			25↑			ns
t <sub>H</sub>	Hold Time (Notes	3, 6)	0↑			0↑			ns
T <sub>A</sub>	Free Air Operatin	g Temperature	-55		125	0		70	°C

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: The symbol  $(\uparrow)$  indicates the rising edge of the clock pulse is used for reference.

Note 4:  $C_L$  = 15 pF,  $R_L$  = 2 k $\Omega$ ,  $T_A$  = 25°C, and  $V_{CC}$  = 5V.

Note 5:  $C_L$  = 50 pF,  $R_L$  = 2 k $\Omega$ ,  $T_A$  = 25°C, and  $V_{CC}$  = 5V.

Note 6:  $T_A$  = 25°C and  $V_{CC}$  = 5V.

#### **Electrical Characteristics**

over recommended operating free air temperature range (unless otherwise noted)

Symbol	nbol Parameter Conditions		Min	Typ (Note 7)	Max	Units	
VI	Input Clamp Voltage	$V_{\rm CC}$ = Min, I <sub>I</sub> = -18 mA				-1.5	V
V <sub>он</sub>	High Level Output	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max	DM54	2.5	3.4		V
	Voltage	V <sub>IL</sub> = Max, V <sub>IH</sub> = Min	DM74	2.7	3.4		
V <sub>OL</sub>	Low Level Output	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max	DM54		0.25	0.4	
	Voltage	V <sub>IL</sub> = Max, V <sub>IH</sub> = Min	DM74		0.35	0.5	V
		$I_{OL}$ = 4 mA, $V_{CC}$ = Min	DM74		0.25	0.4	
l <sub>l</sub>	Input Current @Max	V <sub>CC</sub> = Max	Data			0.1	
	Input Voltage	$V_1 = 7V$	Clock			0.1	mA
			Preset			0.2	1
			Clear			0.2	
I <sub>IH</sub>	High Level Input	V <sub>CC</sub> = Max	Data			20	
	Current	V <sub>1</sub> = 2.7V	Clock			20	μΑ
			Clear			40	1
			Preset			40	1

Electrical	Characteristics	(Continued)
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Symbol	Parameter Conditions		5	Min	Тур	Max	Units
					(Note 7)		
I <sub>IL</sub> L	Low Level Input	V <sub>CC</sub> = Max	Data			-0.4	
	Current	$V_{I} = 0.4V$	Clock			-0.4	mA
			Preset			-0.8	
			Clear			-0.8	
l <sub>os</sub>	Short Circuit	V <sub>CC</sub> = Max	DM54	-20		-100	mA
	Output Current	(Note 8)	DM74	-20		-100	
I <sub>cc</sub>	Supply Current	V <sub>CC</sub> = Max (Note 9)			4	8	mA

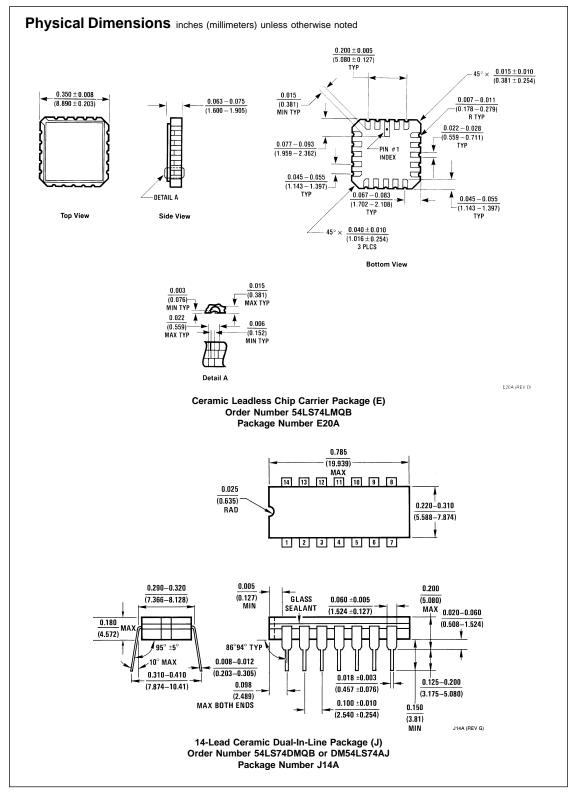
Note 7: All typicals are at V\_{CC} = 5V, T\_A = 25°C.

Note 8: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where  $V_0 = 2.25V$  and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment. Note 9: With all outputs open, I<sub>CC</sub> is measured with CLOCK grounded after setting the Q and  $\overline{Q}$  outputs high in turn.

# Switching Characteristics at V\_{CC} = 5V and T\_A = 25 $^\circ\text{C}$

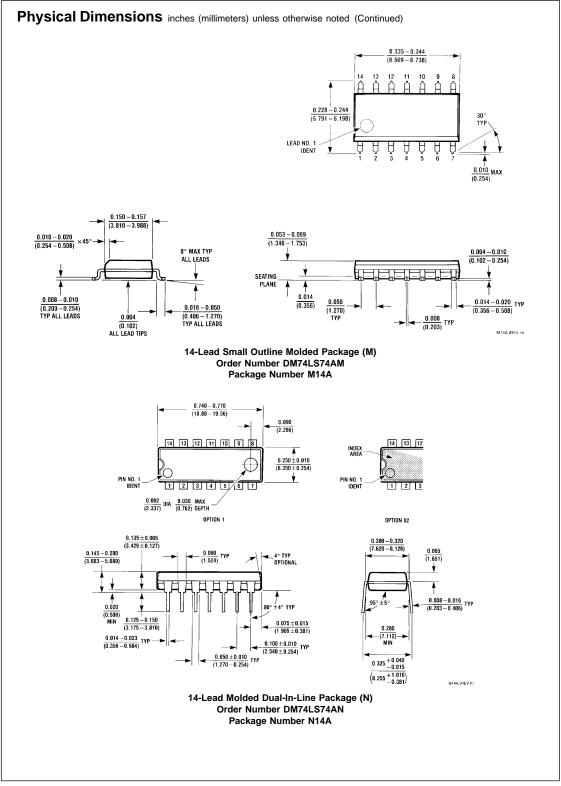
		From (Input)					
Symbol	Parameter	To (Output)	C <sub>L</sub> = 15 pF		C <sub>L</sub> = 50 pF		Units
			Min	Max	Min	Max	]
f <sub>MAX</sub>	Maximum Clock Frequency		25		20		MHz
t <sub>PLH</sub>	Propagation Delay Time	Clock to		25		35	ns
	Low to High Level Output	Q or $\overline{Q}$					
t <sub>PHL</sub>	Propagation Delay Time	Clock to		30		35	ns
	High to Low Level Output	Q or Q					
t <sub>PLH</sub>	Propagation Delay Time	Preset		25		35	ns
	Low to High Level Output	to Q					
t <sub>PHL</sub>	Propagation Delay Time	Preset		30		35	ns
	High to Low Level Output	to Q					
t <sub>PLH</sub>	Propagation Delay Time	Clear		25		35	ns
	Low to High Level Output	to Q					
t <sub>PHL</sub>	Propagation Delay Time	Clear		30		35	ns
	High to Low Level Output	to Q					

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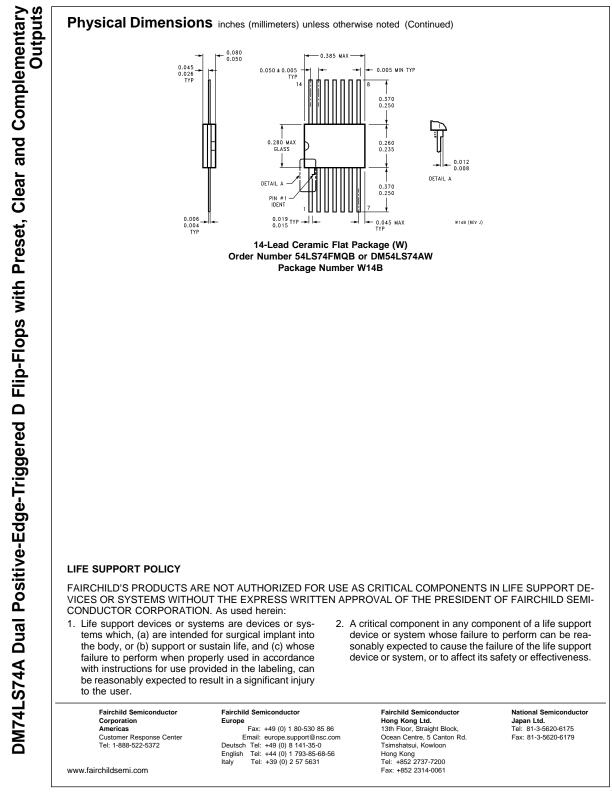


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4



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